WHAT IS CLAIMED IS:

1. A method of evaluating a system-on-a-chip IC (SoC), comprising the following steps of:

building two or more metal layers to establish a pad frame and internal circuit nodes for each core in an SoC while connecting I/O (input and output) pads on a lower metal layer to a top metal layer, thereby exposing all I/O pads and power pads on a surface of the top metal layer of the pad frame of each core; and

applying test vector to each core through the I/O pads on the top metal layer of the core and evaluating response outputs of the core received through the I/O pads on the top metal layer.

2. A method of evaluating a system-on-a-chip (SoC) as defined in Claim 1, wherein the step of building the metal layers of core includes a step of duplicating the internal circuit node in the core to the top metal layer, thereby making accessible of the internal circuit node and the I/O pads by contact probes.

3. A method of evaluating a system-on-a-chip (SoC) as defined in Claim 1, wherein the step of connecting the I/O pads to the top metal layer includes a step of using metal vias between a lower metal layer and an upper metal layer of the pad frame, thereby duplicating the I/O pads toward the top metal layer.

4. A method of evaluating a system-on-a-chip (SoC), comprising the following steps of:

building a chip I/O (input and output) frame at an outer area of an SoC for interfacing with the SoC through contact pads formed thereon;

building two or more metal layers to establish a pad frame and internal circuit nodes for each core in the SoC while connecting I/O pads on a lower metal layer to a top metal layer, thereby exposing all I/O pads and power pads on a surface of the top metal layer of the

pad frame of each core;

applying test vector to the SoC through the contact pads formed on the chip I/O pad frame and evaluating response outputs of the SoC received through the contact pads on the chip I/O pad frame; and

applying test vector to each core through the I/O pads formed on the top metal layer of the core and evaluating response outputs of the core received through the I/O pads on the top metal layer.

5. A method of evaluating a system-on-a-chip (SoC) as defined in Claim 4, wherein the step of building the metal layers includes a step of duplicating the internal circuit node in the core to the top metal layer, thereby making accessible of the internal circuit node and the I/O pads by contact probes.

6. A method of evaluating a system-on-a-chip (SoC) as defined in Claim 4, wherein the step of connecting the I/O pads to the top metal layer includes a step of using metal vias between a lower metal layer and an upper metal layer of the pad frame, thereby duplicating the I/O pads toward the top metal layer.

7. A method of evaluating a system-on-a-chip (SoC) as defined in Claim 4, further comprising the step of removing the I/O pads on the top metal layer of each core.

8. A structure of a system-on-a-chip IC (SoC) for evaluating design integrity thereof, comprising:

a chip I/O (input and output) frame at an outer area of the SoC for interfacing with the SoC through contact pads formed thereon; and

two or more metal layers of a pad frame for each core in the SoC where I/O pads on a lower metal layer are connected to a top metal layer, thereby exposing all I/O pads and power pads on a surface of the top metal layer of the pad frame of each core;

wherein test vectors are applied to the SoC through

the contact pads formed on the chip I/O pad frame to evaluate response outputs of the SoC received through the contact pads on the chip I/O pad frame; and

wherein test vectors are applied to each core through the I/O pads formed on the top metal layer of the core to evaluate response outputs of the core received through the I/O pads on the top metal layer.

9. A structure of a system-on-a-chip IC (SoC) as defined in Claim 8, wherein two or more metal layers include internal circuit nodes in the core which are duplicated to the top metal layer, thereby making accessible of the internal circuit nodes and the I/O pads by contact probes.